CLAIMS

I claim:

1. An assembly for packaging and cooling a semiconductor die comprising:

a substrate;

a semiconductor die mounted on the substrate;

a thermal spreader in heat conducting relation with the semiconductor die on a side of the die opposite the substrate; and

a gasket of a lossy material on the substrate surrounding the die to protect the die from electrostatic discharge pulses.

2. The assembly according to claim 1, wherein the thermal spreader extends beyond the outer peripheral edge of the die and overhangs an adjacent edge of the gasket.

3. The assembly according to claim 1, further comprising a heat sink in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the die.

4. The assembly according to claim 1, wherein the semiconductor die is a microprocessor.

5. The assembly according to claim 1, wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

6. The assembly according to claim 5, wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.

7. The assembly according to claim 1, wherein the gasket is bonded to the substrate with an adhesive.

8. The assembly according to claim 7, wherein the adhesive is conductive.

9. The assembly according to claim 1, wherein the gasket is formed of expanded polytetrafluorethylene material filled with a conductive material to the

extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

10. The assembly according to claim 1, wherein the gasket has a hole therein the size of the die through which the die protrudes.

11. The assembly according to claim 1, wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the assembly is to be used.

12. The assembly according to claim 1, wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz in frequency.

13. An apparatus for increasing the immunity of a microprocessor from electrostatic discharge events comprising:

a substrate;

a microprocessor mounted on the substrate;

a thermal spreader in heat conducting relation with the microprocessor on a side of the microprocessor opposite the substrate;

a heat sink in heat conducting relation with the thermal spreader on a side of the thermal spreader opposite the microprocessor;

a gasket of a lossy material on the substrate surrounding the microprocessor to protect the microprocessor from electrostatic discharge pulses; and

wherein the thermal spreader extends beyond the outer peripheral edge of the microprocessor and overhangs an adjacent edge of the gasket.

14. The apparatus according to claim 13, wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

15. The apparatus according to claim 14, wherein the volume resistivity of the static dissipative material is less than 10^9 ohm cm.

16. The apparatus according to claim 13, wherein the gasket is bonded to the substrate with an adhesive.

17. The apparatus according to claim 13, wherein the gasket is the size of the substrate.

18. The apparatus according to claim 13, wherein the gasket is formed of expanded polytetrafluorethylene filled with a conductive material to the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

19. The apparatus according to claim 13, wherein the gasket has a hole therein the size of the microprocessor through which the microprocessor protrudes.

20. The apparatus according to claim 13, wherein the gasket has a shielding effectiveness to protect the microprocessor from at least 4 kV of electrostatic discharge pulse at a system level in which the apparatus is to be used.

21. The apparatus according to claim 13, wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz in frequency.

22. An electronic package with protection from electrostatic discharge events comprising:

a substrate;

a semiconductor die mounted on the substrate;

a heat sink in heat conducting relation with the semiconductor die on a side of the semiconductor die opposite the substrate; and

a gasket of a lossy material on the substrate surrounding the semiconductor die to protect the die from electrostatic discharge pulses.

23. The electronic package according to claim 22, further comprising a thermal spreader located intermediate the semiconductor die and the heat sink to thermally couple the die and heat sink.

24. The electronic package according to claim 22, wherein the lossy material of the gasket is a static dissipative material having a volume resistivity of greater than 10^2 ohm cm.

25. The electronic package according to claim 22, wherein the gasket is formed of expanded polytetrafluorethylene filled with a conductive material to

the extent that the gasket material has a volume resistivity of greater than 10^2 ohm cm.

26. The electronic package according to claim 22, wherein the gasket has a hole therein the size of the die through which the die protrudes.

27. The electronic package according to claim 22, wherein the gasket has a shielding effectiveness to protect the die from at least 4 kV of electrostatic discharge pulse at a system level in which the electronic package is to be used.

28. The electronic package according to claim 22, wherein the gasket material has a shielding effectiveness of greater than 45 dB up to 3 GHz.

29. A method for increasing the immunity of a microprocessor from electrostatic discharge events comprising:

mounting a microprocessor on a substrate;

surrounding the microprocessor with a gasket formed of lossy, static dissipative material having a volume resistivity of greater than 10^2 ohm cm; and

arranging a heat spreader in heat conducting relation with the

microprocessor and atop at least a portion of the gasket.

30. The method according to claim 29, further comprising adhesively bonding the gasket to the substrate.